07/25/00 17

NEW, CONTINUATION, DIVISIONAL OR CONTINUATION-IN-PART APPLICATION UNDER 37 C.F.R. §1.53(b)

Attorney Docket No. 8693-000221

Express Mail Label No. EL623522854US

Date July 24, 2000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Box Patent Application
Hon. Commissioner of Patents and Trademarks
Washington, D. C. 20231

Sir:

Transmitted herewith for filing under 37 C.F.R §1.53(b) is a patent application for

METHOD AND STRUCTURE FOR REDUCING CAPACITANCE BETWEEN INTERCONNECT LINES

identified by: [ ] First named inventor _____
or [X] Attorney Docket No. (see above)

1. **Type of Application**

[X] This application is a new (non-continuing) application.

[ ] This application is a [ ] continuation / [ ] divisional / [ ] continuation-in-part of prior application No. ____. Amend the specification by inserting before the first line the sentence:

--This is a [continuation/division/continuation-in-part] of United States patent application No. ____, filed ____.--

[ ] The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied, is considered part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

If for some reason applicant has not requested a sufficient extension of time in the parent application, and/or has not paid a sufficient fee for any necessary response in the parent application and/or for the extension of time necessary to prevent the abandonment of the parent application prior to the filing of this application, please consider this as a Request for an Extension for the required time period and/or authorization to charge our Deposit Account No. 08-0750 for any fee that may be due. THIS FORM IS BEING FILED IN TRIPLICATE: one copy for this application; one copy for use in connection with the Deposit Account (if applicable); and one copy for the above-mentioned parent application (if any extension of time is necessary).

2. **Contents of Application**

a. Specification of 12 pages;
[ ] A microfiche computer program (Appendix);
[ ] A nucleotide and/or amino acid sequence submission;

[ ] Because the enclosed application is in a non-English language, a verified English translation [ ] is enclosed [ ] will be filed.

[ ] Cancel original claims ____ of the prior application before calculating the filing fee. (At least one original independent claim must be retained for filing date purposes.)

b. [X] Drawings on 2 sheets;

c. [X] A signed Declaration [X] is enclosed / [ ] will be filed in accordance with 37 C.F.R. §1.53(f).

The enclosed Declaration is [X] newly executed / [ ] a copy from a prior application under 37 C.F.R. §1.63(d) / [ ] accompanied by a statement requesting the deletion of person(s) not inventors in the continuing application.

d. **Fees**

FILING FEE CALCULATION	Number Filed				Number Extra		Rate		Basic Fee $690.00
Total Claims	9	–	20	=	0	×	$18.00	=	0.00
Independent Claims	2	–	3	=	0	×	$78.00	=	0.00
Multiple Dependent Claim(s) Used							$260.00	=	0.00
FILING FEE – NON-SMALL ENTITY									$690.00
FILING FEE - SMALL ENTITY: Reduction by 1/2 [ ] Verified Statement under 37 C.F.R. §1.27 is enclosed. [ ] Verified Statement filed in prior application.									0.00
Assignment Recordal Fee ($40.00)									$40.00
37 C.F.R. §1.17(k) Fee (non-English application)									0.00
TOTAL									**$730.00**

[X] A check is enclosed to cover the calculated fees. The Commissioner is hereby authorized to charge any additional fees that may be required, or credit any overpayment, to Deposit Account No. 08-0750. A duplicate copy of this document is enclosed.

[ ] The calculated fees will be paid within the time allotted for completion of the filing requirements.

[ ] The calculated fees are to be charged to Deposit Account No. 08-0750. The Commissioner is hereby authorized to charge any additional fees that may be required, or credit any overpayment, to said Deposit Account. A duplicate copy of this document is enclosed.

3. **Priority Information**

[ ] **Foreign Priority**: Priority based on _____ Application No. _____, filed _____, is claimed.

[ ] A copy of the above referenced priority document [ ] is enclosed / [ ] will be filed in due course, pursuant to 35 U.S.C. §119(a)-(d).

[ ] **Provisional Application Priority**: Priority based on United States Provisional Application No. ____, filed ____, is claimed under 35 U.S.C. §119(e).

Attorney Docket No. 8693-000221

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4. **Other Submissions**

[ ] A Preliminary Amendment is enclosed.

[ ] An Information Disclosure Statement, ____ sheets of PTO Form 1449, and ____ patent(s)/publications/documents are enclosed.

[X] A power of attorney

[X] is submitted [X] with the new Declaration.

[ ] is of record in the prior application and [ ] is in the original papers / [ ] a copy is enclosed.

[X] An Assignment of the invention

[X] is enclosed with a cover sheet pursuant to 37 C.F.R. §§3.11, 3.28 and 3.31.

[ ] is of record in a prior application. The assignment is to ____, and is recorded at Reel ____, Frame(s) ____.

[ ] An Establishment of Assignee's Right To Prosecute Application Under 37 C.F.R. §3.73(b), and Power Of Attorney is enclosed.

[X] An Express Mailing Certificate is enclosed.

[ ] Other: _____

_____

Attention is directed to the fact that the correspondence address for this application is:

Harness, Dickey & Pierce, P.L.C.
P.O. Box 828
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(248) 641-1600.

Respectfully,

Date July 24, 2000

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Date: July 24, 2000

Box Patent Application
Hon. Commissioner of Patents
and Trademarks
Washington, D.C. 20231

Sir:

EXPRESS MAILING CERTIFICATE

Applicant: Bing-Chang Wu

Serial No (if any):

For: METHOD AND STRUCTURE FOR REDUCING CAPACITANCE BETWEEN INTERCONNECT LINES

Docket: 8693-000221

Attorney: Thomas T. Moga

"Express Mail" Mailing Label Number **EL623522854US**

Date of Deposit ..... **July 24, 2000**

I hereby certify and verify that the accompanying PATENT APPLICATION including acknowledgement postcard, check for $730.00, Transmittal Letter (in triplicate), 12 page patent application (8 pages specification, 3 pages claims, 1 page abstract), Declaration and Power of Attorney (attached to application), two (2) sheets of drawings showing Figures 1-4 and Assignment with required cover sheet (in duplicate) is being deposited with the United States Postal Service "Express Mail Post Office To Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to Box Patent Application, Hon. Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Signature of Person Mailing Document(s)

Method And Structure For Reducing Capacitance Between Interconnect Lines

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method of fabricating an interconnect structure, and more particularly relates to a method of reducing capacitance between interconnect lines and a structure thereof.

2. Description of the Prior Art

Integrated circuits have continued to shrink in size and increase in complexity with each new generation of devices. As a result, integrated circuits increasingly require very close spacing of interconnect lines and many now require multiple levels of metalization, to interconnect the various circuits on the device. Since closer spacing increases capacitance between adjacent lines, as the device geometries shrink and densities increase capacitance, cross talk between adjacent lines becomes more of a problem. Therefore, it becomes increasingly more desirable to use lower dielectric materials to offset this trend and thereby lower capacitance between closely spaced interconnects.

Interconnect capacitance has two components: the line-to - substrate, or line- to- ground capacitance and line- to- line capacitance. For ultra large scale integration at 0.25 μm design rule and beyond,

performance is dominated by interconnect RC delay, with line-to –line capacitance being the dominated contributor to total capacitance. Therefore, a reduction of the line-to-line capacitance alone will provide a dramatic reduction in total capacitance. It becomes increasingly important to implement low K materials between tightly spaced metal lines.

The inter-metal dielectric (IMD) of the prior art is typically SiO_2 which has a dielectric constant of about 4.0. It would be desirable to replace this material with a material having a lower dielectric constant. However, there are many issues existing in the technique of employing low K materials between tightly spaced metal lines, such as mechanical strength , dimensional stability, thermal stability, ease of pattern and etch, thermal conductivity, CMP compatibility and complexity of integration. Many low K materials including polysilsequioxane, parylene, polyimide, benzocyclobutene and amorphous TELFLON all have the above problems, and are inferior to the currently used inter-metal dielectric material SiO_2.

Thus, currently, the most appropriate method to implement low K materials between tightly spaced interconnect lines is utilizing air gaps between interconnect lines. The air gap formation permits the utilization of air as an intra-level dielectric material, which has the relative dielectric constant of 1.0, which is much lower than the relative dielectric constants of other conventional dielectric materials. However, as shown in the drawing of figure 1, the conventional process for forming air gaps in the substrate, having interconnect lines formed thereon, includes depositing an inter-metal dielectric layer 2 over the substrate 1

to form air gaps 3, 4 between the interconnect lines. Due to the spacing between interconnect lines is varied, the spacing is larger, the air gap is formed higher from the substrate 1, such as air gap 4. When subsequently proceeding CMP process for the inter-metal dielectric layer 2, the higher air gap 4 is open up by the CMP process, then such as acid, Alumina will enter into the inter-metal dielectric layer 2 to result in this layer works fail. Moreover, the air gap is formed faster near the lateral wall of the bottom of interconnect lines, the hole of the air gap is tapered from the bottom to the top of the air gap. Thus, the low K effect of the conventional air gap is not well.

Accordingly, it is desired to find out a method for forming air gaps between interconnect lines, to not only reduce capacitance between the interconnect lines, but also overcome the drawbacks of the conventional air gap formation process.

SUMMARY OF THE INVENTION

The primary object of the invention is to provide a method for reducing capacitance between interconnect lines, which forming a pad oxide layer on each of metal lines to form an interconnect line, thereby increase intra-metal aspect ratio to facilitate air gap formation in the spacing between adjacent interconnect lines.

Another object of the invention is to provide a method for reducing capacitance between interconnect lines, which forms a more ideal air gap in the spacing between adjacent metal lines, the upper and lower ends of the air gap respectively exceeding the top and bottom ends

of the adjacent metal lines, and the distance from the portion of air gap between the top and bottom ends of the metal line to the sidewall of the metal line is more consistent and smaller, so as to minimize difference of low K effect of the portion of air gap, and give better low K effect.

A further object of the invention is to provide a method for reducing capacitance between interconnect lines, which forms a pad oxide layer on each of metal lines to form an interconnect line, so that an air gap is formed in the spacing between the adjacent interconnect lines under the top end of the pad oxide layer. Therefore, the air gap is not damaged while proceeding subsequent CMP process.

A still further object of the present invention is to provide an interconnect structure for reducing capacitance between interconnect lines, which is characterized in that each of air gaps in the spacings of adjacent interconnect lines each of which comprising a lower metal line and a upper pad oxide layer is formed below the top end of the pad oxide layer with more consistent and smaller spacing between the air gap and the sidewall of the metal line.

In order to achieve the above objects of this invention, the present invention provides a method and structure for reducing capacitance between interconnect lines comprising: providing a substrate having a plurality of semiconductor elements and one dielectric layer for isolating the semiconductor elements formed thereon. Forming a metal layer over the substrate; and then forming a pad oxide layer over the metal layer. Subsequently, patterning and etching the metal layer and pad oxide layer to constitute interconnect lines over the

substrate. Thereafter, forming an inter-metal dielectric layer over the substrate having the interconnect lines. Thereby, a plurality of air gaps are respectively formed in the spacings between the adjacent interconnect lines, having larger aspect ratios. Finally, planarizng the inter-metal dielectric layer by chemical mechanical polishing method.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention itself, however, as well as features and advantages thereof, will be best understood by reference to the detailed description of one embodiment which follows, read in conjunction with the accompanying drawings, wherein:

FIG. 1 shows a cross-sectional view of air gaps formed in the spacing between the adjacent interconnect lines in the prior art;

FIG. 2 shows a cross-sectional view of a substrate having a metal layer and a pad oxide layer sequentially formed thereon, for one embodiment of the present invention;

FIG. 3 shows a cross-sectional view of the substrate of FIG. 2, wherein interconnect lines have constituted thereon; and

FIG. 4 is a cross-sectional view of depositing an inter-metal dielectric layer over the structure of FIG. 3, in which a plurality of air gaps are respectively formed in each of the spacings between the adjacent interconnect lines having larger aspect ratios.

DESCRIPTION OF THE EMBODIMENT

Referring to FIG. 2, the present invention firstly providing a substrate 5, having a plurality of semiconductor elements and one dielectric layer for isolating the semiconductor elements formed thereon (not shown in the figure); depositing a metal layer 6 over the substrate 5, the metal layer 6 can be an aluminum layer deposited by DC sputtering deposition method, about 3000~10000 angstronm thickness, the metal layer 6 also can be formed by metals selected from the group consisting of Cu, Ta, Au, Pb, Si, W and Sn; then depositing a pad oxide layer 7 over the metal layer 6 with thickness between about 2000 angstronm and about 5000 angstronm, the pad oxide layer 7 can be a SiO_2 layer, deposited by atmospheric pressure CVD method, utilizing SiH_4 as reaction gas, under the pressure of 0.5~1 torr, at temperature of 400~500℃. Alternatively, deposited by plasma enhanced CVD method, utilizing SiH_4 as reaction gas, under the pressure of 1~10 torr, at temperature of 300~400℃. Otherwise, deposited by plasma enhanced CVD method, utilizing TEOS/O3 as reaction gas.

Referring to FIG. 3, subsequently, patterning and etching the pad oxide layer 7 and metal layer 6 by the conventional lithography and etching technique to constitute adjacent interconnect lines 8.

Referring to FIG. 4, thereafter, depositing an inter-metal dielectric layer 9 over the substrate 5 having adjacent interconnect lines 8 formed thereon. Since the pad oxide layer 7 formed on each of metal lines 6 increases intra-metal aspect ratio between the adjacent interconnect lines 8, a plurality of air gaps, such as air gaps 10, 11, are

respectively formed in each of the spacings between the adjacent interconnect lines 8 having larger aspect ratios. Furthermore, as shown in figure 4, the distance from the portion of the air gaps 10 and 11 between the top end and bottom end of the metal line 6 to the respective sidewall of the metal lines 6 is more consistent and smaller. Hence, the difference of low K effect in the spacing between the adjacent metal lines 6 is minimized, and a better low K effect is obtained.

The inter-metal dielectric layer 9 formed over the substrate 5 can be a SiO_2 layer, deposited by plasma enhanced CVD method, utilizing TEOS/O_3 as reaction gas. Besides, the inter-metal dielectric layer 9 can also be a BPSG layer, deposited by atmospheric pressure CVD method, utilizing TEOS/O_3, TMPO (tri-methyl-phosphate) and TEB (tri-methyl-borate) as reaction gas, at the temperature less than 550℃. Otherwise, the BPSG layer can be formed by plasma enhanced CVD method, utilizing TEOS, O_3/O_2, TMP and TMB as reaction gas, at temperature between about 400℃ and about 500℃. However, the content of Boron is controlled in about 1~4 weight %, while the content of Phosphorus is controlled in about 6~8 weight %. Finally, the inter-metal dielectric layer 9 is planarized by chemical mechanical polishing method (CMP), to build up another level of metalization.

To sum up the foregoing, the present invention provides a method for air gap formation that a pad oxide layer is formed on each of metal lines to form interconnect lines having increasing aspect ratios. Thereby, a more ideal air gap is formed in the spacing between the adjacent interconnect lines, in which the portion of air gap between the top end and bottom end of the metal lines is more uniformly formed than

that formed by the conventional air gap formation process. Therefore, the present invention provides better low K effect in the spacing between the adjacent metal lines. Additionally, the air gap is formed between the adjacent interconnect lines under the top end of the pad oxide layer, so that subsequent CMP process does not open up the air gap.

In accordance with the present invention, it is apparent that there has been provided an improved method of reducing capacitance between adjacent interconnect lines which overcomes the disadvantages of the prior art. The present invention is inexpensive and uncomplicated, can easily be integrated into conventional process flows without significantly increasing cycle time, maintains heat transfer efficiency through the interconnect structure, and is compatible with reducing the size of semiconductor integrated circuits.

Although one specific embodiment has been illustrated and described, it will be obvious to those skilled in the art that various modifications may be made without departing from what is intended to be limited solely by the appended claims.

CLAIMS

What is claimed is:

1. A method for reducing capacitance between interconnect lines, the method comprising:

providing a substrate having a plurality of semiconductor elements and one dielectric layer for isolating the semiconductor elements formed thereon;

forming a metal layer over said substrate;

forming a pad oxide layer over said metal layer;

pattering and etching said pad oxide layer and metal layer to constitute said interconnect lines over said substrate;

forming an inter-metal dielectric layer over said substrate having said interconnect lines formed thereon, wherein at least an air gap is formed in a spacing between the adjacent interconnect lines; and

planarizing said inter-metal dielectric layer.

2. The method according to claim 1, wherein said metal layer is formed from materials selected from the group consisting of Al, Cu, Ta, W, Si, Au, Pb and Sn.

3. The method according to claim 1, wherein the thickness of said pad oxide layer is between about 2000 angstronm and about 5000 angstronm.

4. The method according to claim 1, wherein said pad oxide layer comprises SiO_2, deposited by atmospheric pressure CVD method.

5. The method according to claim 1, wherein said pad oxide layer comprises SiO_2, deposited by plasma enhanced CVD method.

6. The method according to claim 1, wherein said inter-metal dielectric layer comprises a SiO_2 layer, deposited by plasma enhanced CVD method, utilizing TEOS/O3 as reaction gas.

7. The method according to claim 1, wherein said inter-metal dielectric layer comprises a BPSG layer, deposited by atmospheric pressure CVD method, utilizing TEOS/O_3, TMPO and TEB as reaction gas, at temperature lower than 550℃.

8. The method according to claim 1, wherein said inter-metal dielectric layer comprises a BPSG layer, deposited by plasma enhanced CVD method, utilizing TEOS, O_3/O_2, TMP and TMB as reaction gas, at temperature between about 400℃ and 500℃.

9. An interconnect structure, the structure comprising:

a substrate having a plurality of semiconductor elements and one dielectric layer for isolating the semiconductor elements formed thereon;

a plurality of adjacent interconnect lines having spacings therebetween with different aspect ratios with at least an air gap formed therein formed over said substrate, each of which comprising a lower metal line and a top pad oxide layer, said air gap is positioned below said pad oxide layer and the level of the top end of said air gap is beyond the upper ends of said adjacent metal lines, and the level of the lower

end of said air gap is below the bottom ends of said adjacent metal lines; and

an inter-metal dielectric layer formed over said substrate having said adjacent interconnect lines formed thereon.

Method And Structure For Reducing Capacitance Between Interconnect Lines

ABSTRACT OF THE INVENTION

A method and structure for reducing capacitance between interconnect lines, characterized in that a pad oxide layer is added on each of metal lines over a substrate, having a plurality of semiconductor elements and one dielectric layer for isolating the semiconductor elements formed thereon, to form an interconnect line. The pad oxide layer added on each of metal lines increases intra-metal aspect ratio and facilitates air gap formation in each of the spacings between the adjacent interconnect lines having larger aspect ratios. Moreover, each of air gaps is formed below the pad oxide layer, while the top end and lower end thereof respectively exceed the top end and bottom end of the adjacent metal lines. The distance from the portion of the air gap between the top end and bottom end of the adjacent metal lines to the sidewall of the adjacent metal lines is more consistent and smaller. Therefore, a better low K effect between the adjacent metal lines is obtained.

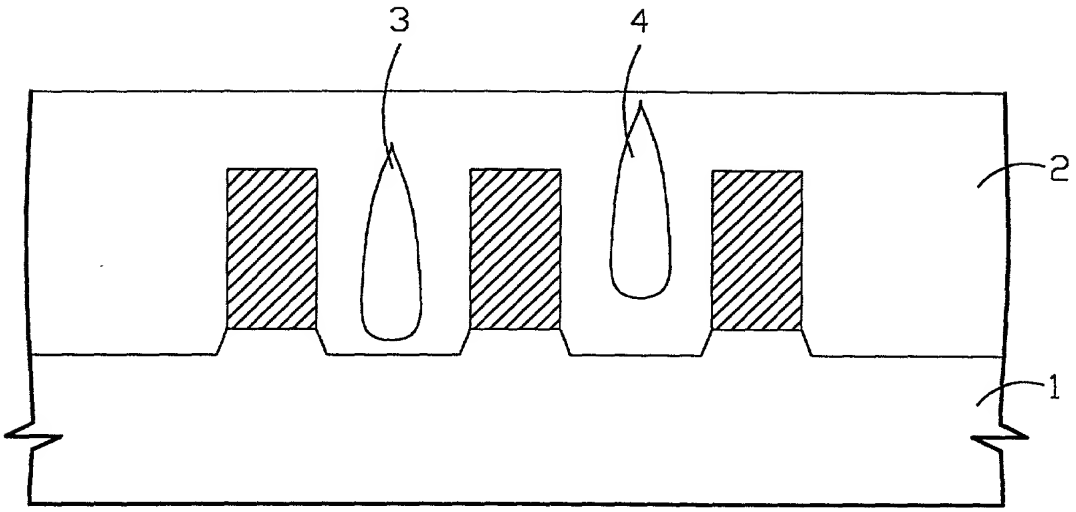

FIG.1(Prior Art)

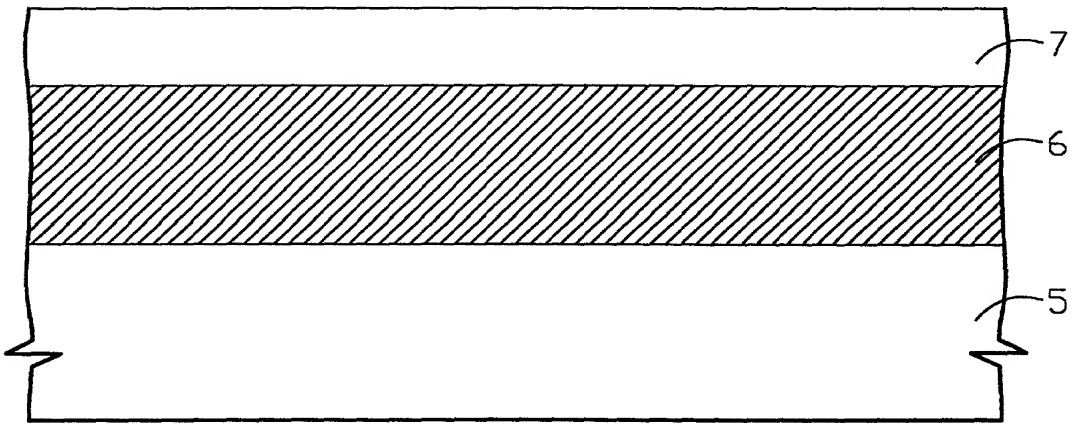

FIG.2

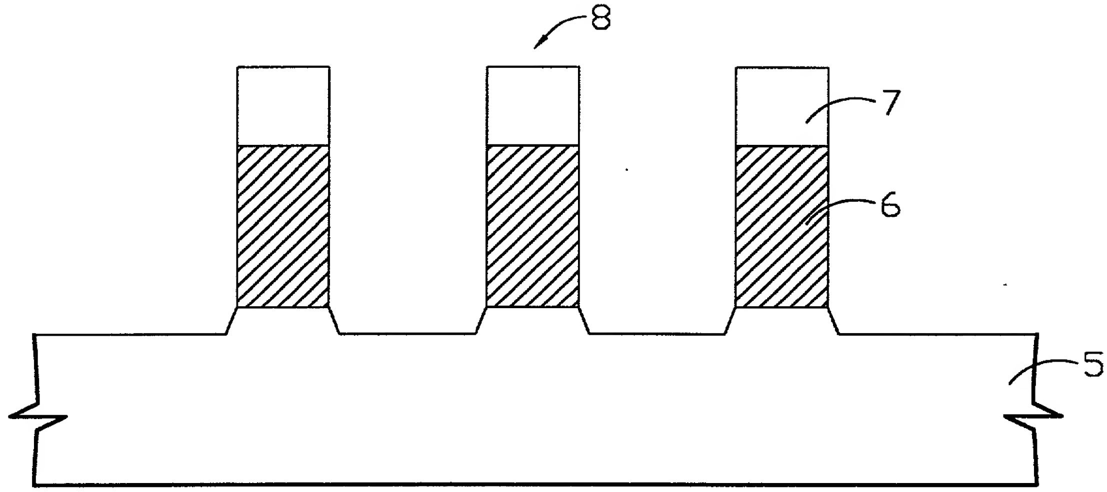

FIG.3

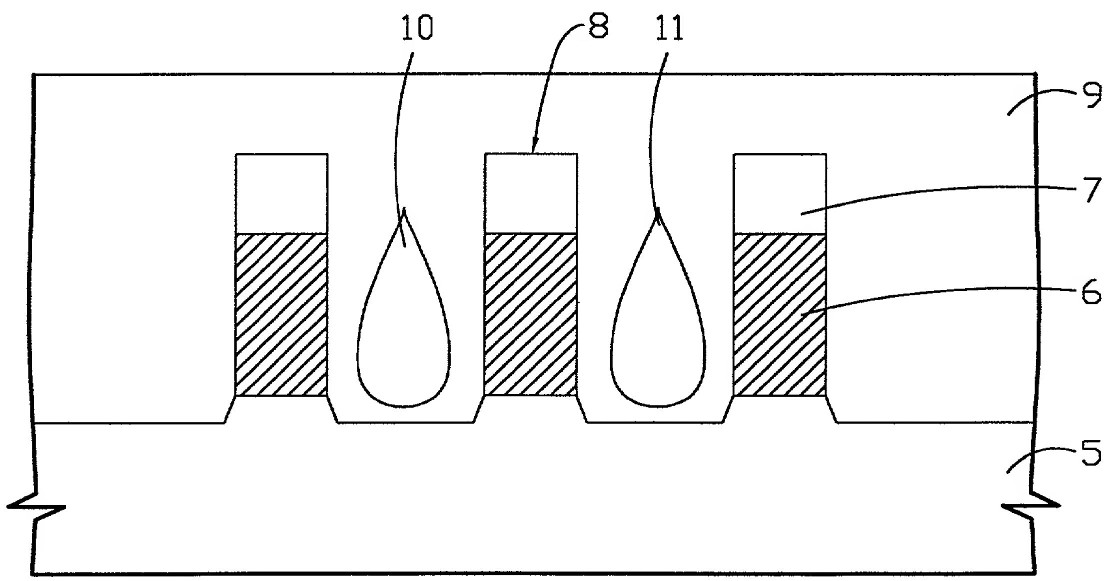

FIG.4

Attorney Docket No. 8693-000221

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD AND STRUCTURE FOR REDUCING CAPACITANCE BETWEEN INTERCONNECT LINES

The specification of which (check one)

[x] is attached hereto.

[ ] was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty of disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, section 119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

			Priority Claim	
(Number)	(Country)	(Day/Month/Year filed)	Yes	No
(Number)	(Country)	(Day/Month/Year filed)	Yes	No
(Number)	(Country)	(Day/Month/Year filed)	Yes	No

DECLARATION AND POWER OF ATTORNEY

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States Provisional application(s) listed below:

PRIOR PROVISIONAL APPLICATIONS

(application serial number)	(Month / Day / Year filed)
(application serial number)	(Month / Day / Year filed)

I hereby claim the benefit under Title 35, United States Code, section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United Sates application in the manner provided by the first paragraph of Title 35, United States Code, section 112. I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	**Filing Date**	**Status – patented, pending, abandoned**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint Thomas T. Moga, Reg. No. 34,881, and each principal, attorney of counsel, associate and employee of Harness, Dickey & Pierce, P.L.C., who is a registered Patent Attorney, my attorney with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith. I request the Patent and Trademark Office to direct all correspondence and telephone calls relative to this application to Harness, Dickey & Pierce, P.L.C., P.O. Box 828, Bloomfield Hills, Michigan 48303 (248) 641-1600.

Full name of sole or first inventor: Bing-Chang WU

Inventor's signature: Bing Chang Wu

Date: JUL 14 2000

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